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| EXAMINER | |
|---|---|
| CHANG, EDITH M | |
| **ART UNIT** | **PAPER NUMBER** |
| 2637 | |

DATE MAILED: 07/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/737,370 | DAVIS, KEVIN C. | |
| | Examiner | Art Unit | |
| | Edith M. Chang | 2637 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *23 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Continued Examination Under 37 CFR 1.114*

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on May 23, 2005 has been entered.

### *Information Disclosure Statement*

2. The listing of references in the specification is not a proper information disclosure statement. 37 CFR 1.98(b) requires a list of all patents, publications, or other information submitted for consideration by the Office, and MPEP § 609 A(1) states, "the list may not be incorporated into the specification but must be submitted in a separate paper." Therefore, unless the references have been cited by the examiner on form PTO-892, they have not been considered.

"The prior art tap circuit design Hewlett Packard 3787B DS1 interface" is listed in page 8 lines 14-20, however is not in the IDS, hence it has not been considered.

***Response to Arguments/Remarks***

3. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

***Claim Objections***

4. Claims 2-14 and 20 are objected to because of the following informalities:

Claim 2, line 1: "the circuitry" should be "the impedance load circuitry"; line 2: "the circuitry" should be "the amplifying circuitry"; line 3: "the circuitry" should be "impedance matching circuitry".

Claim 3, line 1: "the circuitry" should be "the impedance load circuitry".

Claim 4, line 1: "further comprising" should be "the impedance load circuitry further comprising". Since the transmission line tap circuit of Fig.1 comprises impedance load circuitry ($R_1$ to $R_4$ and $C_1$ to $C_4$ directly connected to the amplifying circuitry), amplifying circuitry and impedance matching circuitry, two input terminals and two output terminals, and the impedance load circuitry comprises two resistors and two capacitors, each resistor and capacitor is connected to one of the input terminals respectively as disclosed in Fig.1. The transmission line tap circuit does not additionally comprise circuitry (capacitor connected to the input terminal) to block direct current present in the received transmission signal.

Claims 6 & 8, line 1: "further comprising" should be "the impedance load circuitry further comprising".

Claim 7, line 3: "resistors connected in series and coupled to the at least two input terminals" should be changed to "resistors connected in series at one end of each of the two resistors toge and the other end of each of the two resistors coupled to the at least two input terminals". Since "resistors connected in series" does not clearly indicate that the two resistors ($R_3$ & $R_4$) connected in series in one end to the ground, as the invention described in the specification and disclosed in the drawing, and "resistors connected in series" is ambiguous to point out the subject matter.

Claim 10, line 1: "the circuitry" should be "the amplifying circuitry".

Claim 11, line 1: "further comprising" should be "the impedance matching circuitry further comprising". Since the transmission line tap circuit of Fig.1 comprises impedance load circuitry, amplifying circuitry and impedance matching circuitry ($R_8$, $R_9$, $C_7$ and $C_8$ directly connected to a plurality of outputs of the amplifying circuitry), two input terminals and two output terminals, and the impedance matching circuitry comprises two resistors and two capacitors, each resistor and capacitor is connected to one of the output terminals respectively as disclosed in Fig.1. The transmission line tap circuit does not additionally comprise circuitry (two resistors parallel to the amplifying circuitry) to provide a dissipation load; line 2: "the circuitry" should be "the amplifying circuitry".

Claim 12, line 2: "the circuitry" should be "the amplifying circuitry".

Claim 13, line 1: "further comprising" should be "the impedance matching circuitry further comprising"; line 2: "the circuitry" should be "the amplifying circuitry".

Claim 20, line 5: "such means" should be changed to "the means for amplifying"; line 9: "the impedance match" should be changed to "the means for providing an impedance match".

Claims 5, 7, 9 and 14 are dependent on the objected claims 4, 6, 8 and 13.

Appropriate correction is required.

### *Claim Rejections - 35 USC § 112*

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 7, 12, 14 and 17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 7, line 3: "resistors connected in series and coupled to the at least two input terminals" does not clearly indicate the configuration arrangement of the two resistors disclosed in the drawing ($R_3$ & $R_4$), wherein one end of each resistor connected together to the ground that in theory the two resistors are parallel connected not series connected. Since "resistors connected in series" does not clearly indicate that the two resistors ($R_3$ & $R_4$) connected in series in one end together to the ground, as the invention described in the specification and disclosed in the drawing, and "resistors connected in series" is ambiguous fail to point out the subject matter.

Claim 12, line 3: "two resistors connected in series" does not clearly

indicate the configuration arrangement of the two resistors disclosed in the drawing, wherein one end of each resistor connected together to the ground that in theory the two resistors are parallel connected not series connected.

Claim 14, line 2: "two capacitors connected in series" does not clearly indicate the configuration arrangement of the two capacitors disclosed in the drawing, wherein one end of each capacitor connected together to the ground that in theory the two capacitors are parallel connected not series connected.

Claim 17, the "gain adjustment circuitry" does not clearly indicate that the "gain adjustment circuitry" is the amplifiers of the amplifying circuitry of the transmission line tap circuit, or the transmission line tap circuit has another (further) circuitry to adjust the gain of the circuit not shown in the disclosure of the drawings of the current specification.

### *Claim Rejections - 35 USC § 103*

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-14 and 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over McEwan (US 5,519,342).

Regarding **claims 1, 18 & 20**, in FIG.6 (column 4 lines 5-7), McEwan

discloses a transient digitizer (the transmission line tap circuit) with displacement current samplers (213s & 217s); at least *two input terminals* (to two sample gates 213) that each input terminal connected to one sampler gate (213 of FIG.6) of one sampling gate circuit, wherein one sampling gate circuit as one set of sampler gate 213, amplifier 217 and the associated elements of FIG.6; *amplifiers* 217s; and two *output terminals* (inputs of 220) coupling the transmission signal to the multiplexer 231 (as the line interface unit used to recover the digital data) to recover the data received. However, FIG.6 does not show the detail associate elements of the samplers 231 and amplifiers 217 to load balance and match for the proper operations of the transient digitizer.

In FIG.8, McEwan teaches an alternative current sampler of each current sampler in FIG.6 (column 4 lines 12-14), wherein the sampler 351 (with the associated elements) of FIG.8 performs the function of the sample gate 213 (with its associated elements) of FIG.6; the amplifier 375 with the FET buffer 368 and associate elements performs the function of amplifier 217 and the 217's associate elements of FIG.6. At the time of the invention was made, it would have been obvious to one of ordinary skill in the art to replace each sample gate 213, amplifier 217 and the associated elements (refer to as a sampling gate circuit) of FIG.6 with the alternative one (sampler 351, FET buffer 368, amplifier 375 and the associate elements) in FIG.8 to have a short transient sampler (column 10 lines 36-44).

The modified/combined transient digitizer comprises a transmission line 212 (column 8 lines 41-45, or 350 of FIG.8), at least *two input terminals* (to the

sample gates 213, the tap 352 of FIG.8) that each input terminal connected to one sampler gate (351 of FIG.8) of one current sampler, wherein one current sampler has one set of sampler gate 213, amplifier 217 and the associated elements of FIG.6 or one set of sampler 351, gate FET 368, amplifier 375 and associated elements shown in FIG.8. The current sampler is connected/tapped to the transmission line (212 FIG.6) and connected to multiplexer 220 to output matching circuit 224 and its associated elements;

a circuitry of the at least two samplers 351, the two associated FET buffers 368, the two associated switches 374 and the associated elements (the associated elements include resistors 361 & 358, capacitor 365, resistor 366, 367, 369, 370, 371 and capacitors 372 & 373 for connecting to each amplifier 375, as the *impedance load* circuitry) of a first and a second sampling gate circuits, tapping the transmission line 350 and receiving the signal transmitted/propagated in the line 350 (column 10 lines 53-55, wherein the sampler 351 provides impedance load);

the at least two operational amplifier buffers 375 FIG.8 of the first and second sampling gate circuit directly connected to a circuitry: the capacitors 218, the amplifier 224 and the associated elements of 224 (as the *impedance matching load*, FIG.6) including feedback capacitor 225, feedback resistor 226 and resistors 227 & 229, directly connected to the outputs of operational amplifiers (217 FIG.6 or 375 FIG.8);

and at least *two output terminals* (inputs of 220) coupling the transmission signal to the multiplexer 231 (as the line interface unit used to recover the digital data) to recover the data received.

The transient digitizer of FIG.6 modified with the alternative current sampler of FIG.8 has a short transient sampler (column 10 lines 36-44) and enables a significant reduction in component count (column 3 lines 30-34).

Regarding **claim 2**, in FIG.6 and FIG.8 (detail of sample gate 213 and charger amplifier 217, column 8 lines 44-45 & lines 53-54), McEwan teaches the at least two samplers 351, the at least two associated FET buffers 368, the at least two associated switches 374 and the associated elements (as the *impedance load* circuitry, the associated elements include resistors 361 & 358, capacitor 365, resistor 366, 367, 369, 370, 371 and capacitors 372 & 373) as the impedance load circuitry, the amplifiers 375 (217 FIG.6) and the capacitors 218, the amplifier 224 and its associated elements (as the *impedance matching load*, FIG.6) including feedback capacitor 225, feedback resistor 226 and resistors 227 & 229 are in one single printed circuit board (column 8 lines 21-23).

Regarding **claims 3 & 6**, the combined/modified McEwan digitizer teaches the circuitry to provide impedance load to the transmission line including one resistor 367 of the first sampler connected to one input terminal and the resistor 367 of the second sampler connected to another input terminal, wherein the resistors as dissipation load to vary the signal inputted to the amplifier 375.

Regarding **claims 4 & 5**, in FIG.6 and FIG.8, McEwan teaches the capacitor 373 of one sampling gate circuit (one circuit of sampler 351, gate FET 368, amplifier 375 and associated elements shown in FIG.8) connected to receive the signal on line 366 to block the direct current in (as shown in the FIG.8).

Regarding **claim 7**, in FIG.8, McEwan teaches the resistor 369 of the first sampling gate circuit connected to the resistor 369 of the second sampling gate circuit in series (to the ground, resistor is dissipation load) and coupled to the two input terminals (352 of each sampling gate circuit FIG.8).

Regarding **claim 8**, in FIG.8, McEwan teaches the capacitor 372 to suppress the high frequency noise ($1/j\omega C$, $\omega$ is the frequency, C is the capacitance of 372) and shape the signal provided to the amplifier 375.

Regarding **claim 9**, in FIG.8, McEwan teaches the capacitor 372 of the first and second sampling gate circuit coupled to respective input terminal (352).

Regarding **claim 10**, in FIG.8, McEwan teaches two amplifiers (one in the first sampling gate circuit, the other on in the second sampling gate circuit) having respective feedback resistors (377), and capacitor (376) paralleled to the feedback resistor.

Regarding **claims 11-12 & 17**, in FIG.6, McEwan teaches the resistor 229 of the output amplifying circuit (as the gain adjustment circuitry, column 9 lines 20-25, the amplifier 224 and its associated elements: 225, 226, 227 and 229), which performs the load matching, and the resistors 226 and 229 connected in series.

Regarding claims **13** & **14**, in FIG.6, McEwan teaches the capacitor 218 to block direct current from the amplifier and coupled to the output terminals.

Regarding **claim 19**, in FIG.6 and FIG.8, McEwan teaches the capacitor 373 of one sampling gate circuit (one set of sampler gate 213, amplifier 217 and the associated elements of FIG.6 or one circuit of sampler 351, gate FET 368, amplifier 375 and associated elements shown in FIG.8) connected to receive the signal on line 366 to block the direct current in (as shown in the FIG.8); and McEwan teaches the resistor 369 of the first sampling gate circuit connected to the resistor 369 of the second sampling gate circuit in series (to the ground, resistor is dissipation load) and coupled to the two input terminals (352 of each sampling gate circuit FIG.8).

9. Claims 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over McEwan (US 5,519,342) in view of Song (US 4,087,754).

Regarding **claims 15** & **16**, McEwan does not specify the T1 or E1 transmission line, however, Song teaches the well-known compressed pulse (CPCM) provided in T1 format (T1 line, same apply to E1 format, column 6 lines 46-48 '754). As the application of McEwan's digitizer providing precise pulse compression (column 3 lines 53-56), at the time of the invention was made, it would have been obvious to one of the ordinary skill in the art to have the T1 format signal transmitted on the signal line 211 of FIG.6 or 350 of FIG.8 to have a plurality of sample gates on a transmission line (column 3 lines 53-56 '342) to provide a tapped transmission line architecture which provides a robust and

simple design (column 2 lines 61-67 '342) for the pulse/code format of the audio/telephone communication (column 1 lines 25-31 '754).

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Edith M. Chang whose telephone number is 571-272-3041. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay K. Patel can be reached on 571-272-2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Edith Chang
July 6, 2005

YOUNG T. TSE
PRIMARY EXAMINER